UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,164	05/05/2005	Matthias Muth	DE02 0252 US	9960

24738 7590 11/15/2006

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER	
ZAMAN, FAISAL M	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/534,164	MUTH, MATTHIAS	
	Examiner	Art Unit	
	Faisal Zaman	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the "black boxes" in Figure 1 should be accompanied with text labels describing what each "black box" is. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: --INTEGRATED CIRCUIT WITH BIT-RATE DETECTION AND SERIAL/PARALLEL CONVERSION CAPABILITIES--.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Feuerstraeter et al. ("Feuerstraeter") (U.S. Patent Application Publication No. 2003/0058894) in view of Applicant's Admitted Prior Art (hereinafter "AAPA") and Ishikuri (U.S. Patent No. 6,674,681).

Regarding Claim 1, Feuerstraeter teaches an integrated circuit having

A system base chip (Feuerstraeter, Figure 3, item 340) that has basic functions for a transmitting and/or receiving system for a data bus, namely at least a monitoring function (Feuerstraeter, Figure 7, item 700),

An interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte (Feuerstraeter, Page 4, paragraphs 0044 and 0047),

A serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit (Feuerstraeter, Figure 3, items 350/360, Page 3, paragraph 0037).

Feuerstraeter does not expressly teach wherein the data bus is a vehicle data bus that uses a LIN (Local Interconnect Network) protocol,

A system voltage supply, and

A system reset.

In the same field of endeavor (e.g. an integrated chip for transmitting/receiving data over a data bus), AAPA teaches the use of a vehicle data bus that uses a LIN protocol (AAPA, Page 1, lines 9-12).

Also in the same field of endeavor (e.g. transmitting and receiving data in an integrated circuit), Ishikuri teaches an integrated circuit having a system voltage supply (Ishikuri, Figure 1, item 1, Column 5, lines 43-56), and

A system reset (Ishikuri, Column 5, lines 57-60).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined AAPA's teachings of an integrated chip for transmitting/receiving data over a data bus with the teachings of Feuerstraeter, for the purpose of allowing compatibility with automotive systems and to provide a small and low-cost bus system. It also would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Ishikuri's teachings of transmitting and receiving data in an integrated circuit with the teachings of

Feuerstraeter, for the purpose of preventing erroneous operations due to runaway of a system (see Ishikuri, Column 5, lines 6-8).

Regarding Claim 6, Feuerstraeter does not expressly teach wherein the serial/parallel converter converts serial data conforming to the SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface standard into parallel data, or vice versa.

In the same field of endeavor, AAPA teaches the use of an SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface (AAPA, Page 1, lines 13-17).

The motivation that was used in the combination of Claim 1, super, applies equally as well to Claim 6.

5. **Claims 2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Feuerstraeter in view of AAPA and Ishikuri as applied to claim 1 above (hereinafter "FAI"), and further in view of Bongiorno et al. ("Bongiorno") (U.S. Patent No. 6,292,045).

Regarding Claim 2, Feuerstraeter teaches an oscillator that acts as a clock-signal source and as a timebase for the bit-rate detection (Feuerstraeter, Figure 3, items 480/490, Page 4, paragraph 0044).

Feuerstraeter does not expressly teach wherein the oscillator is an R/C oscillator.

In the same field of endeavor (e.g. electrical circuits which use clock sources), Bongiorno teaches the use of an R/C oscillator (Bongiorno, Column 1, lines 16-21).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Bongiorno's teachings of electrical circuits which use clock sources with the teachings of FAI, for the purpose of providing an RC oscillator which has the ability to generate high frequency oscillations having a stable frequency characteristic.

Regarding Claim 3, Bongiorno teaches wherein the clock signal generated by the R/C oscillator may also be provided to circuits outside the integrated circuit, and in particular to a microprocessor (Bongiorno, Column 1, lines 16-21).

The motivation that was used in the combination of Claim 2, super, applies equally as well to Claim 3.

6. **Claims 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over FAI, and further in view of Werle (U.S. Patent No. 5,778,002).

Regarding Claims 4 and 5, Feuerstraeter does not expressly teach wherein the interface circuit may also pass on complete messages and perform buffer-storage of data received or to be transmitted.

In the same field of endeavor (e.g. multiplexing asynchronous high-speed and low-speed data into a single data stream for recordation), Werle teaches wherein an interface circuit may pass on complete messages by performing buffer-storage of data received or to be transmitted (Werle, Figure 1, item 14, Column 3, lines 13-27).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Werle's teachings of multiplexing asynchronous high-speed and low-speed data into a single data stream for recordation with the teachings of FAI, for the purpose of reducing latency of the system if the incoming data rate is slower than that which can be processed.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Key et al. (U.S. Patent No. 5,008,902 A) discloses automatic baud rate detection. Mejia (U.S. Patent No. 6,680,970 B1) discloses statistical methods and systems for data rate detection for multi-speed embedded clock serial receivers. Prihadi et al. (U.S. Patent Application Publication No. 2004/0054835 A1) discloses a precision oscillator for an asynchronous transmission system. Baumgartner (U.S. Patent No. 6,771,694 B1) discloses speed negotiation for serial transceivers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

fmz

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100